REMARKS

Claims 7-22 are pending in this application. Claims 1-6 are cancelled. By this Amendment, claims 7 and 8 are amended to correct a grammatical error and to rearrange the claim language as requested by the Patent Office.

Applicant appreciates the courtesies shown to Applicant's representative by Examiner Isaac in the December 12, 2005 personal interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

In view of the foregoing amendments and the following remarks, reconsideration of this application is respectfully requested.

I. Rejection Under 35 U.S.C. §102

Claims 7-22 were rejected under 35 U.S.C. §102(a)/(e) as allegedly being anticipated by U.S. Patent No. 6,362,076 ("Inazuki"). This rejection is respectfully traversed.

Claims 7 and 8, as amended, recite a method of producing an SOI wafer that includes a step of forming an insulator film on at least one of a bond wafer made of silicon single crystal to form an SOI layer and a base wafer made of silicon single crystal to be a support substrate, wherein the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer.

As discussed during the interview, it is important to use a base wafer as recited in claims 7 and 8 to reduce Crystal Originated Particles (COPs) when producing an SOI wafer. As shown in Figure 4 and as explained on page 6, paragraph 3 of the specification, when the SOI layer and the insulator film were made thin, COPs existing in the base wafer had been detected as COPs existing in the SOI layer. Moreover, as shown in Figure 5 and as explained on page 7, paragraph 1 of the specification, the insulator film and the base wafer could not be bonded in the region where the COPs existed, resulting in a micro void.

Thus, when an SOI wafer is produced using the base wafers recited in claims 7 and 8, such SOI wafer hardly has COPs existing near a surface of the base wafer. Even if the insulator film and the SOI are thinner, no more than a few COPs due to the base layer are detected after the SOI wafer was completed, and thus measurements precisely reflecting the number of COPs in the SOI layer can be performed. In addition, a high quality SOI wafer wherein generation of micro voids at an interface between the base wafer and the insulator film is suppressed can be produced. See page 8, paragraph 2 of the specification.

Inazuki teaches a hydrogen iron delamination method for fabricating an SOI wafer that includes preparing two silicon mirror polished wafers, one to be a base wafer and the other to be a bond wafer, subjecting the bond wafer to thermal oxidation so as to form an oxide film having a thickness of about 0.1 μm to 2.0 μm on the surface thereof, implanting at least one of hydrogen ions and rare gas ions into one surface of the bond wafer on which oxide film is formed, and superposing the base wafer on the hydrogen ion-implanted surface of the hydrogen ion-implanted bond wafer via the oxide film. See Inazuki, column 4, lines 46-66.

As discussed during the interview, the method of producing an SOI wafer as recited in claims 7 and 8 clearly distinguishes over Inazuki because nowhere does Inazuki teach or suggest that the base wafer is one silicon wafer selected from a group consisting of an epitaxial wafer, an FZ wafer, a nitrogen doped wafer, a hydrogen annealed wafer, an intrinsic gettering wafer, a nitrogen doped and annealed wafer, and an entire N-region wafer.

The Patent Office alleges that Inazuki teaches that an epitaxial wafer or an FZ wafer is used as the base wafer by citing Figure 1, column 5, lines 17-27 and column 6, lines 39-45 of Inazuki. Such characterization is incorrect. As discussed during the interview, Figure 1 of Inazuki shows the steps of fabricating an SOI wafer, and does not indicate at all that an epitaxial wafer or an FZ wafer is used as the base wafer. Furthermore, at column 5, lines 17-

27 only describe the steps of a bonding heat treatment having certain heat treatment conditions, and at column 6, lines 39-45, an epitaxial wafer or an FZ wafer is used as the bond wafer.

Additionally, as discussed during the interview, Inazuki only teaches that a silicon mirror polished wafer is used as the base wafer. See Inazuki, column 4, lines 45-51. Again, nowhere does Inazuki teach or suggest using an epitaxial wafer, an FZ wafer and the like as a base wafer as recited in claims 7 and 8 in the present application.

Moreover, as described on page 5, paragraph 2 and paragraph 3 of the present specification, a high quality SOI wafer could not be obtained in the past. Because the base wafer supported an SOI layer via an insulator layer, no element was formed directly on the base layer surface. Thus, a wafer having COPs on its surface or a dummy-grade silicon wafer of which resistivity and the like do not meet production standards, was used as a base wafer. That is, the base wafers as recited in claims 7 and 8 have never been used as a base wafer to be a support substrate, even though it has been used as a bond wafer to form an SOI layer. Nowhere does Inazuki teach or suggest an SOI wafer produced by the method as recited in claims 7 and 8, that is, detecting COPs existing in the base wafer as COPs existing in the SOI layer, and that the insulator film and the base wafer could not be bonded in the region in which the COPs existed, resulting in a micro void. In addition, nowhere does Inazuki teach or suggest a method as recited in claims 7 and 8 that produces a high quality SOI wafer that, even where an insulator film and an SOI layer are formed to be thinner in the SOI wafer, COPs are hardly detected in inspection of the SOI layer after the SOI wafer was completed and thus measurements that precisely reflect a number of COPs in the SOI layer can be performed. Thus, the method as taught by Inazuki cannot produce an SOI wafer as claimed.

For all the foregoing reasons, Applicant respectfully submits that Inazuki fails to anticipate the subject matter of claims 7 and 8, and claims dependent therefrom. Reconsideration and withdrawal of this rejection are respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 7-22 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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